

# **BIPOLAR AND CMOS INTEGRATION WITH REDUCED CONTACT HEIGHT**

## **BACKGROUND OF THE INVENTION**

### *Field of the Invention*

[0001] The present invention generally relates to integrated circuit structures that include multiple height devices and more particularly to an improved structure that reduces the height of the passivating layer to reduce the height of the contacts made to such devices.

### *Description of the Related Art*

[0002] Fabrication of BiCMOS chips (integrated circuit chips having both bipolar transistors and complementary metal oxide semiconductor (CMOS) transistors) requires process integration of both bipolar and CMOS field effect transistors (FET) devices. One of the key challenges in process integration is to make contact connections to the differently sized devices. Reliable contact connection has always been one of the significant issues for base CMOS FET fabrication. Due to the significant vertical height difference between bipolar and CMOS FET devices, contact formation becomes even more difficult for BiCMOS chip fabrication. At present, the aspect ratio of contacts for BiCMOS is about 30% higher than base CMOS for 0.25 and 0.18 $\mu$ m SiGe technologies. This aspect ratio difference becomes unsustainable for future SiGe technologies (e.g., 0.13 $\mu$ m or below). The present invention described below provides a reliable solution to contact formation for future BiCMOS technologies.

## SUMMARY OF THE INVENTION

**[0003]** The invention provides a method of forming different devices on a substrate. More specifically, the invention forms a plurality of complementary metal oxide semiconductor (CMOS) transistors and vertical bipolar transistors on the substrate. Note that the vertical bipolar transistors are taller than the CMOS transistors. The invention deposits a passivating layer over the bipolar transistors and the CMOS transistors and then removes a portion of the passivating layer so as to expose the vertical bipolar transistors and leave the CMOS transistors covered by the passivating layer. Next, the invention forms contacts to the CMOS transistors through the passivating layer and forms a wiring layer above the passivating layer such that the wiring layer is in direct contact with the vertical bipolar transistors.

**[0004]** Prior to forming the wiring layer the invention can form emitter contacts above the vertical bipolar transistors. These emitter contacts are actually positioned within the wiring layer, and can be made of a different material than the wiring within the wiring layer. The invention can also form a via layer above the wiring layer. The emitter contacts will extend through the wiring layer to the via layer. This process also forms base and collector contacts to the vertical bipolar transistors.

**[0005]** The inventive processing produces an integrated circuit structure that includes a plurality of complementary metal oxide semiconductor (CMOS) transistors and a plurality of vertical bipolar transistors positioned on a single substrate. The vertical bipolar transistors are taller devices than the CMOS transistors and can extend more than twice as far above the substrate as the CMOS transistors. In this structure, a passivating layer is positioned above the substrate and between the vertical bipolar transistors and the CMOS transistors. A wiring layer is above the passivating layer. The vertical bipolar transistors are in direct contact with the wiring layer and the CMOS transistors are connected to the wiring layer by contacts extending through the passivating layer.

**[0006]** There is also a via layer above the wiring layer and the vertical bipolar transistors emitter contacts are directly connected to the via layer. The emitter contacts extend through the wiring layer to the via layer. Thus, the emitter contacts are positioned within the wiring layer

and can comprise a different material than the wiring within the wiring layer. Base and collector contacts connecting base and contact regions of the vertical bipolar transistors to the wiring layer extend through the passivating layer.

[0007] The invention polishes the BPSG very close to the top of bipolar device to decrease the contact opening aspect ratio and correspondingly decrease contact defect rates. The invention uses a wider emitter contact for the bipolar devices. Thus, the invention provides easier contact connection integration (more reliable contacts and better yield) and faster bipolar transistors with reduced lateral dimension.

[0008] These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0009] The invention will be better understood from the following detailed description with reference to the drawings, in which:

[0010] Figure 1 is a schematic diagram of structure that includes multiple devices having different heights;

[0011] Figure 2 is a schematic diagram of a partially completed structure;

[0012] Figure 3 is a schematic diagram of a partially completed structure;

[0013] Figure 4 is a schematic diagram of a partially completed structure;

[0014] Figure 5 is a schematic diagram of a partially completed structure;

[0015] Figure 6 is a schematic diagram of structure that includes multiple devices having different heights; and

[0016] Figure 7 is a flow diagram illustrating a preferred method of the invention.

## **DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION**

**[0017]** The present invention and the various features and advantageous details thereof are explained more fully with reference to the nonlimiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

**[0018]** Figure 1 illustrates an integrated circuit that includes multiple devices 116, 118 that have different heights. In the examples used herein, the devices include a CMOS transistor 116 and a vertical bipolar transistor 118. However, the invention is not limited to these specific devices and these devices are selected in these examples merely to illustrate the operation of the invention. Therefore, the invention is equally applicable to any integrated circuit structure that incorporates devices of different sizes into its design. For example, the invention is equally applicable to any combination of a horizontal device and a vertical device or differently sized horizontal and/or vertical devices. The invention can be used with bipolar transistors, varactors, diodes, field effect transistors, resistors, capacitors, etc. Moreover, the present invention can also be applied to the formation of FET contacts such as gate and source or drains should the topography difference between FET contacts become a severe constraint to manufacturing fabrication.

**[0019]** In Figure 1, item 110 represents a substrate such as a silicon substrate upon which the devices 116, 118 are formed. Item 112 illustrates an insulator passivation layer that could be formed from, for example, Boron Phosphor doped Silicate Glass (BPSG) or other similar substance. Items 114 illustrate various contacts (e.g., polysilicon, metal, alloy, etc.) that are made

through the passivation layer 112. Item 120 represents a wiring layer with various first metal layer (M1) wires 122. The emitter contact of the vertical bipolar transistor 118 is shown as item 124 in Figure 1. Item 126 represents an insulator that separates the wiring layer 120 from the passivating layer 112. A via/wiring layer 132 includes first level vias (V1) 130 and additional second metal layer (M2) wires 134. Item 128 represents an insulator that separates the first metal layer 120 from the second metal/via layer 132.

[0020] The structure shown in Figure 6 is different than that shown in Figure 1 in that, in the structure shown in Figure 6, the emitter contact 124 is positioned within the wiring layer 120 instead of below the wiring layer 120 (as in the structure shown in Figure 1). This allows the passivating layer 112 to be shorter in Figure 6 than in Figure 1 which, in turn, decreases the aspect ratio of the remaining contacts 114, thereby substantially reducing the defect rate of the contacts 114. In addition, the width of the emitter contact 124 can be made larger with the structure shown in Figure 6 because the emitter contact is formed using a dedicated mask exclusive to the emitter contact. By making the emitter contact wider the margin of positioning error is made greater and the width of emitter itself can be fabricated narrower. In other words, by making the emitter contact wider, the possibility of defects resulting from misalignment of the emitter and its contact decreases. This allows the emitter to be made smaller without increasing the probability of a misalignment-type defect. It is well known that a narrower emitter can lead to smaller parasitic capacitance and hence substantially increase the switching speed of the bipolar transistor 118.

[0021] Figures 2-5 illustrate processing steps leading up to the structure shown in Figure 6. More specifically, Figure 2 illustrates the structure just after the passivating layer 112 is formed. Conventional processes reduce the raw height of the passivating film 112 down to level 202, thereby removing a portion shown by arrow 200. This can be performed, for example, in a standard chemical mechanical polishing (CMP) process, or similar processing. However, as shown in Figure 3, the invention reduces the height of the passivating layer 112 down to the level indicated by arrow 300 which is approximately equal to the top of the tallest device 302 (which, in this example, is the top of the vertical bipolar transistor 118). For example, the height of the passivating layer 112 could be reduced to within approximately (plus or minus) 50 nanometers of

the top of the tallest device 118. To the contrary, Figure 2 stops polishing at a much higher level (e.g., 400 nanometers) above the tallest devices.

[0022] Figure 3 also illustrates the contacts 114 to the collector and based terminals of the critical bipolar device 118 and to the source, drain, and gate of the transistor 116 formed using standard damascene metal processing. For example, the contacts 114 can be formed from polysilicon, metal, alloy, etc. (e.g., tungsten). As explained above, the reduced height of the passivating layer 112 reduces the aspect ratio of the contacts 114, which dramatically decreases contact related defects (e.g., electrically open contacts, etc.). As a result, higher yields and more reliable contacts are produced with the invention.

[0023] As shown in Figure 4, the invention optionally forms a dielectric 126 (e.g., silicon nitride, silicon carbide, etc.) and a lower dielectric constant material, undoped silicate oxide, etc. 120 as the insulating portion of the first wiring layer (M1). A dedicated photolithographic mask is used to pattern openings for the emitter contact 124 in the wiring layer 120. The emitter contact 124 comprises polysilicon, or a metal such as tungsten, etc. This processing allows the size and width of the emitter contact 124 to be independently controlled from all other processing. Because this mask is not shared, over-etching of the emitter is reduced. If the emitter contact and other deeper contacts are fabricated together with a shared mask, there is a significant over-etching of the emitter contact because the plasma etch reaches the bottom of emitter contact first and continues etching to open deeper contacts. By making the emitter contact wider, the width of emitter itself can be fabricated narrower. It is well known that narrower emitter can lead to smaller parasitic capacitance, and hence, substantially increase the switching speed of the bipolar transistor 118.

[0024] As shown in Figure 5, a separate mask is used to form openings in the insulator 120 in which wires 122 will be formed. The wiring material 122 is deposited in the openings and the excess is removed in a standard CMP process. Such wires 122 are generally metal, such as copper, aluminum, etc. Therefore, the emitter contact 124 can be made of a different material than the wires 122. Preferably, the emitter contact 124 is made of a material compatible with the CMP processing that will be performed on the wiring material 122.

**[0025]** This structure is completed as shown in Figure 6 through the formation of the second wiring/via layer 132. More specifically, an additional insulator 128 similar to insulator 126 can be formed followed by a lower dielectric constant material 132. Multiple damascene processes are used to pattern openings and fill the openings with the vias 130 and wires 134 in a similar manner to that discussed with respect to wires 122.

**[0026]** Thus, the invention provides a method of forming different devices on a substrate. In the example shown above, the invention forms a plurality of complementary metal oxide semiconductor (CMOS) transistors 116 and vertical bipolar transistors 118 (only one of each is illustrated) on the substrate 110. Note that the vertical bipolar transistors 118 are taller than the CMOS transistors 116. The invention deposits a passivating layer 112 over the bipolar transistors 118 and the CMOS transistors 116 and then removes a portion of the passivating layer 112 so as to expose the vertical bipolar transistors 118 and leave the CMOS transistors 116 covered by the passivating layer 112. Next, the invention forms contacts 114 to the CMOS transistors 116 through the passivating layer 112 and forms a wiring layer 120 above the passivating layer 112 such that the wiring layer 120 is in direct contact with the vertical bipolar transistors 118.

**[0027]** Prior to forming the wiring layer 120, the invention can form emitter contacts 124 above the vertical bipolar transistors 118. These emitter contacts 124 are actually positioned within the wiring layer 120, but can be made of a different material than the wiring 122 within the wiring layer 120. The invention can also form a via layer 132 above the wiring layer 120. The emitter contacts 124 can extend through the wiring layer 120 to the via layer 132. This process also forms base and collector contacts 114 to the vertical bipolar transistors 118.

**[0028]** Figure 7 illustrates this processing in flowchart form. More specifically, in item 700, the invention forms a plurality of devices (e.g., complementary metal oxide semiconductor (CMOS) transistors and vertical bipolar transistors) on the substrate. The invention deposits a passivating layer 702 over the bipolar transistors and the CMOS transistors and then removes a portion of the passivating layer 704 down to the top of the vertical bipolar transistors. This leaves the CMOS transistors covered by the passivating layer. Next, the invention forms contacts 704 to the CMOS transistors through the passivating layer. The invention can form

emitter contacts 706 above the vertical bipolar transistors and form a wiring layer 708 above the passivating layer such that the wiring layer is in direct contact with the vertical bipolar transistors. The invention can also form a via layer 710 above the wiring layer.

**[0029]** The invention polishes the BPSG very close to the top of bipolar device to decrease the contact opening aspect ratio and correspondingly decrease contact defect rates. The invention uses a wider emitter contact for the bipolar devices. Thus, the invention provides easier contact connection integration (more reliable contacts and better yield) and faster bipolar transistors with reduced lateral dimension (e.g., the width of the Bipolar device can be reduced due to less over-etching during emitter contact RIE etch).

**[0030]** While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.